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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/658,700	09/09/2003	Shigetaka Kasuga	10873.1269US01	2313

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EXAMINER	
PRABHAKHER, PRITHAM DAVID	
ART UNIT	PAPER NUMBER
2622	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	12/29/2006	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/658,700	KASUGA ET AL.	
	Examiner	Art Unit	
	Pritham Prabhakher	2622	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09/09/2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Specification

The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

The disclosure is objected to because of the following informalities:

On Page 3, Lines 26 and 27, the vertical scanning circuit should be numbered 205, and the horizontal scanning circuit should be numbered 206.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-4 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Koizumi et al. (US Patent No.: 7129985B1) and further in view of Yonemoto et al. (US Patent No.: 6483541B1) and Mutoh et al. (A 1v Multi-Threshold Voltage CMOS DSP with an Efficient Power Management Technique for Mobile Phone Application).

In regard to ***Claim 1****, Koizumi et al. teach of an imaging device chip set comprising:*

an imaging chip provided for obtaining an electric signal by photoelectric conversion of incident light (Looking at Figure 23, 210 represents the imaging chip with the image sensor for obtaining an electric signal by photoelectric conversion of incident light); and

a DSP chip provided for carrying out digital signal processing with respect to the electric signal obtained by the imaging chip (214 in Figure 23, shows a DSP chip for carrying out signal processing),

wherein the imaging chip includes:

a pixel unit for generating the electric signal by the photoelectric conversion of incident light (Looking at Figure 12, the reference shows a pixel unit of an image sensor);

a horizontal scanning circuit for selecting the unit pixels in a horizontal direction (See 1c in Figure 12); and

a vertical scanning circuit for selecting the unit pixels in a vertical direction (See 1b in Figure 12),

the DSP chip includes:

a timing generating circuit for generating timing pulses necessary for operations of the horizontal scanning circuit and the vertical scanning circuit (Looking at the DSP chip 214 in Figure 23, the clock control 215 is the timing generating circuit for generating timing pulses); and

a digital signal processing circuit for carrying out digital signal processing with respect to the electric signal generated by the plurality of unit pixels (Figure 23 shows

that a DSP 217 (DSP circuit) is present for carrying out signal processing with respect to the electric signal generated by the image sensor 212),

Although Koizumi et al. teach of a pixel unit, the reference does not specifically teach of a plurality of pixel units. The reference also does not teach that the plurality of unit pixels, the horizontal scanning circuit, and the vertical scanning circuit, which are included in the imaging chip, are formed with transistors of a same conductivity type. Yonemoto et al. teach of a large number of pixel transistors (pixel units) that are of the same conductivity type (NMOS transistors), ***Figure 1 and Column 10 Lines 12-14 of Yonemoto et al.)****. It would have been obvious to one of ordinary sill in the art at the time of the invention to incorporate multiple pixel units of the same conductivity type into the teachings of Koizumi et al. because this would provide a better image while making it easier to correct for noise since the noise patterns from the pixel units would appear fixed after the capturing of an image.*

Koizumi et al. and Yonemoto et al. also do not disclose that the timing generating circuit and the digital signal processing circuit, which are included in the DSP chip, are formed with CMOS transistors. Mutoh et al. teach of forming a timing generating circuit and DSP circuit using CMOS transistors, ***Page 1, Line 1 et seq. and Figures 1, 2 and 5 of Mutoh et al****. It would have been obvious to one of ordinary skill in the art at the time of the invention to form a timing generating circuit and DSP circuit using CMOS transistors since they help reduce power consumption,* ***Page 1, Line 1 et seq. of Mutoh et al.)****.*

*In regard to **Claim 2**, Koizumi et al. , Yonemoto et al. and Mutoh et al. disclose the imaging device chip set according to claim 1,*

*wherein the plurality of unit pixels, the horizontal scanning circuit, and the vertical scanning circuit, which are included in the imaging chip, are formed with n-MOS transistors (Yonemoto et al. teach that the unit pixels, the horizontal scanning circuit and the vertical scanning circuit are formed with NMOS transistors, **Column 10, Lines 12-14 of Yonemoto et al.)**.*

*With regard to **Claim 3**, Koizumi et al. , Yonemoto et al. and Mutoh et al. do not specifically disclose the imaging device chip set according to claim 1, wherein the transistors of the same conductivity type that form the plurality of unit pixels, the horizontal scanning circuit, and the vertical scanning circuit, which are included in the imaging chip, are formed according to a minimum dimension greater than a minimum dimension for forming the CMOS transistors that form the timing generating circuit and the digital signal processing circuit included in the DSP chip.*

However, official notice is taken that it would have been obvious and well known at the time of the invention that the CMOS transistors used in the DSP chip are smaller in size than NMOS transistors used in the Image Sensor because a principle well known advantage of CMOS over NMOS is lower power consumption. Therefore, the transistors with CMOS technology are smaller in size than the ones implementing NMOS technology.

*In regard to **Claim 4**, Koizumi et al., Yonemoto et al. and Mutoh et al. disclose the imaging device chip set according to claim 1, wherein at least a part of the*

horizontal scanning circuit and vertical scanning circuit included in the imaging chip is formed with dynamic logic circuits (Koizumi et al. teach that horizontal scanning circuit and the vertical scanning circuit included in the imaging chip are formed with dynamic logic (MOS) circuits, ***Figure 6 of Koizumi et al.)****.*

Regarding ***Claim 8****, Koizumi et al., Yonemoto et al. and Mutoh et al. disclose the imaging device chip set according to claim 1, wherein each of the unit pixels included in the imaging chip includes an embedded-type photodiode that is formed so as to be exposed on a surface of a substrate (The buried photo diode is formed in the substrate surface of the n-type region,* ***Column 6, Lines 20-25 of Koizumi et al.)****.*

Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Koizumi et al. (US Patent No.: 7129985B1), Yonemoto et al. (US Patent No.: 6483541B1), Mutoh et al. (A 1v Multi-Threshold Voltage CMOS DSP with an Efficient Power Management Technique for Mobile Phone Application). as applied to claim 1 above, and further in view of Ewedemi et al. (US Patent No.: 6985181B2)

Regarding ***Claim 5****, Koizumi et al., Yonemoto et al. and Mutoh et al. disclose the imaging device chip set according to claim 1,*

wherein the imaging chip further includes:

an amplifier circuit (Operational amplifier 24, ***Column 10, Lines 59-61 of Yonemoto et al.)*** *for amplifying the electric signal generated by the plurality of unit pixels.*

However, Koizumi et al., Yonemoto et al., and Mutoh et al. do not disclose an analog-digital converting circuit for converting the electric signal amplified by the amplifier circuit into a digital signal and feeding the digital signal to the digital signal processing circuit included in the DSP chip. Ewedemi et al. teach of an image sensor that has an A/D converter. It would have been obvious to one of ordinary skill in the art to incorporate an A/D converter into the image-sensing chip of Koizumi et al. because converting an amplified, analog image signal to digital allows it to be read out at a much higher speed, ***Column 4, Lines 29-37 of Ewedemi et al.***

Claims 6 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Koizumi et al. (US Patent No.: 7129985B1), Yonemoto et al. (US Patent No.: 6483541B1), Mutoh et al. (A 1v Multi-Threshold Voltage CMOS DSP with an Efficient Power Management Technique for Mobile Phone Application)., Ewedemi et al. (US Patent No.: 6985181B2) as applied to claims 1 and 4 above, and further in view of Suda (US Patent No.: 6441441B1)

In regard to ***Claims 6 and 7****, Koizumi et al., Yonemoto et al., Mutoh et al., and Ewedemi et al. do not specifically disclose the imaging device chip set according to claim 4 wherein the plurality of transistors forming the dynamic logic circuits are isolated from one another with thick oxide films formed on a substrate, and that the plurality of transistors forming the dynamic logic circuits are isolated from one another with ion-implanted layers, the ion-implanted layers being formed so as to be exposed on a surface of a substrate.*

Suda teaches of transistors being isolated from one another by the element isolating oxide films, ***Column 1, Lines 49-43 of Suda****. It would have been obvious to one of ordinary skill in the art at the time of the invention to isolate the transistors of Yonemoto et al. from each other via the means of oxide films taught by Suda, because this serves as a protective film for each surface of the layers of the semiconductor,* ***Column 2, Lines 62-65 of Suda****.*

In regard to the isolation of the transistors from one another with ion-implanted layers which are formed to be exposed on the surface of the substrate, official notice is taken deeming that it would have been obvious to isolate the transistors with ion-implanted layers because this is an old and well known way of creating separation among the transistors which prevents crosstalk and leakage currents.

Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Koizumi et al. (US Patent No.: 7129985B1), Yonemoto et al. (US Patent No.: 6483541B1), Mutoh et al. (A 1v Multi-Threshold Voltage CMOS DSP with an Efficient Power Management Technique for Mobile Phone Application). as applied to claim 1 above, and further in view of Miyamoto (US Patent No.: 6518999B1)

In regard to ***Claim 9****, Koizumi et al., Yonemoto et al., and Mutoh et al. disclose an image pickup system comprising:*

the imaging device chip set according to claim 1;

a memory that stores function information for executing functions (See memory 229 in Figure 23 of ***Koizumi et al.****); and*

a controller for reading out the function information stored in the memory, and feeding the function information to the DSP chip provided in the imaging device chip set (The system control unit 228 in Figure 23 of ***Koizumi et al.)****.*

However, Koizumi et al., Yonemoto et al., and Mutoh et al. do not disclose that the memory executes functions including an electronic shutter and an automatic diaphragm. Miyamoto teaches of an electronic shutter that inherently has an automatic diaphragm, ***Column 4, Line 12 of Miyamoto.*** *It would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate an electronic shutter into the teachings of Koizumi et al., Yonemoto et al., and Mutoh et al. because this increases the continuous shooting speed of the camera in which the image sensor is present,* ***Column 1, Line 23 of Miyamoto.***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Pritham Prabhakher whose telephone number is 571-270-1128. The examiner can normally be reached on M-F (7:30-5:00) Alt Friday's Off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Ometz can be reached on (571)272-7593. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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